

REMARKS

Applicants respectfully request reconsideration and withdrawal of the rejection of the claims. Claims 1-8, 10-24 and 26-40 currently are pending.

Claim 1 has been amended to recite that the comparison circuit operates to receive the reference clock signal and compares a phase of a signal having the phase and frequency of the reference clock signal with a phase of a signal having a frequency that is twice that of the comparison signal. In claim 21, the step of generating has been amended to recite: “generating the phase difference signal by comparing a phase of a signal having the phase and frequency of the reference clock signal with a phase of a signal having a frequency that is twice that of the comparison signal.” Favorable reconsideration is respectfully requested in view of the following remarks.

In the most recent Office Action, claims 1-8 and 21-24 were rejected under 35 U.S.C. § 112, first paragraph, as allegedly failing to comply with the enablement requirement. This rejection is respectfully traversed.

In setting forth the rejection, the Examiner asserts that the recitation of claim 1: “a comparison circuit that receives the reference clock signal and compares a phase of the reference clock signal with a phase of a signal having a frequency that is twice that of the comparison signal,” was not supported in the original disclosure in such a way that one skilled in the art would not be enabled to make and/or use the invention. The Examiner reasons that the specification, at page 10, line 22 to page 12, line 12, and Figure 6 do not disclose the reference clock signal being received at points where phases of signals are compared. It is respectfully submitted, however, that such interpretation mischaracterizes broadly recited features of comparing *phases* of a reference clock and another signal having twice the frequency of the received comparison signal. These claimed features do not necessarily recite that the actual reference clock signal is compared at some point in the comparison circuit with another signal. Rather, it is the *phase* of the reference clock signal that is compared, which is not necessarily conveyed in a comparison of the actual clock signal, as alleged by the Examiner. For example, Figure 8 shows an example in which the phase information of the reference signal is embodied in the source signal that is output from

flip-flop 601, and this phase is compared with the phase of the signal having a frequency that is twice the frequency of the comparison signal (e.g., the sink signal having a frequency that is twice the f_{feedback} “comparison” signal) by way of the charge pump. It is respectfully submitted that one of ordinary skill in the art would have understood how to make and/or use the claimed invention from what is described in the original disclosure.

Similar arguments apply to the rejection of claim 21, which the Examiner objected to for reciting the language “directly comparing a phase of the reference clock signal with a phase of a signal having a frequency that is twice that of the comparison signal.” In the statements of the rejection, the Examiner alleges that the phases of the two compared signals are not directly compared because the specification describes two charge pump signals being compared and not the direct comparison of the phases of the reference and comparison signals. It is respectfully submitted, however, that the triggering of the charge pumps of the example of the invention mentioned in the Action does represent a direct comparison of a *phase* of a reference clock signal with a *phase* of a signal (e.g., a feedback signal) having a frequency that is twice that of a comparison signal, within a reasonable interpretation of “directly” as claimed, because a rising (or falling) edge of a reference clock signal triggers the charge pump source current (e.g., see Figure 8).

However, to advance this application to allowance, Applicants have amended claims 1 and 21 to make the meaning of the comparing features recited in these claims abundantly clear. For instance, claim 1 has been amended to recite that the comparison circuit operates to compare *a phase of a signal having the phase and frequency of the reference clock signal*. A similar amendment has been made to claim 21. See the examples of Figures 5-8 and the text related thereto for support of these changes. It is respectfully submitted that these amended features as recited in combination with the other recitations of claims 1 and 21 fully meet the enablement requirement under Section 112, first paragraph.

Hence, Applicants respectfully submit that independent claims 1 and 21 are allowable.

Because independent claims 1 and 21 are allowable, it is respectfully submitted that dependent claims 2-8 and 22-24 also are allowable.

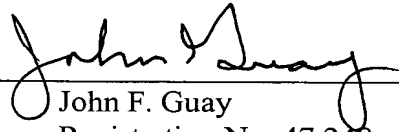
In light of the foregoing, Applicants respectfully request reconsideration and withdrawal of the rejection of claims 1-8, 10-24 and 26-40.

Respectfully submitted,

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